

FIG. 1A

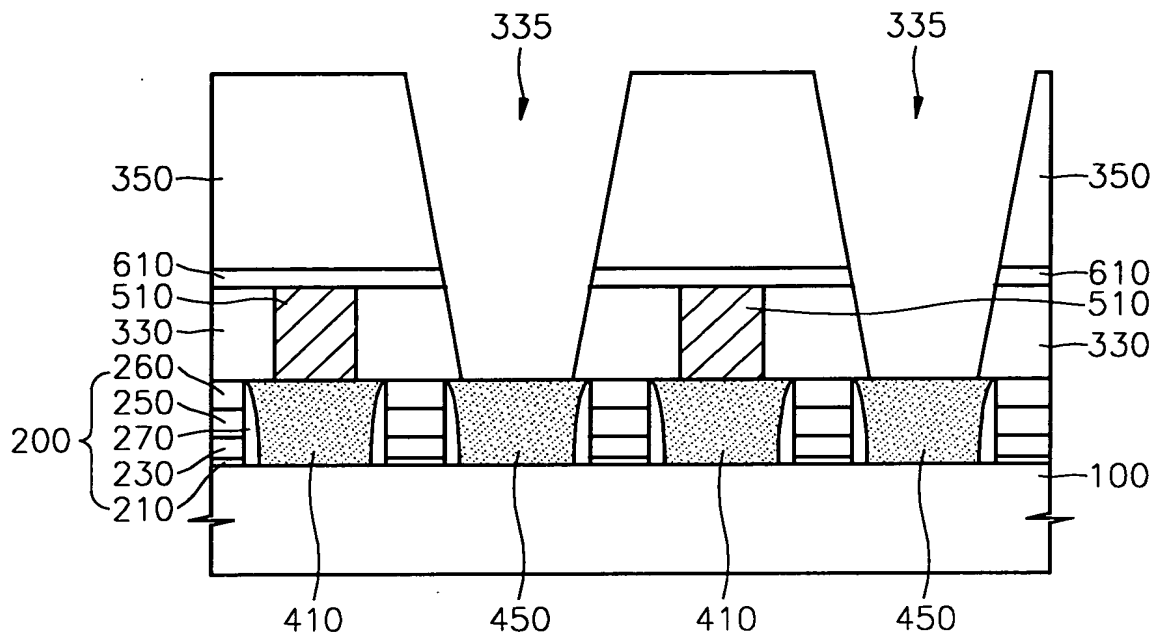


FIG. 1B

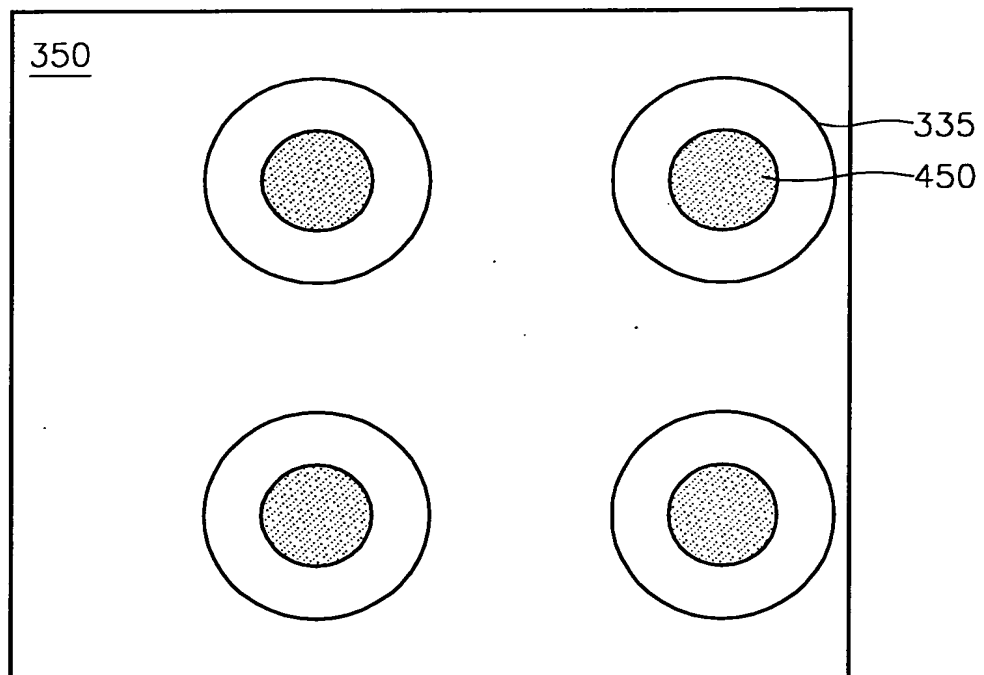


FIG. 2

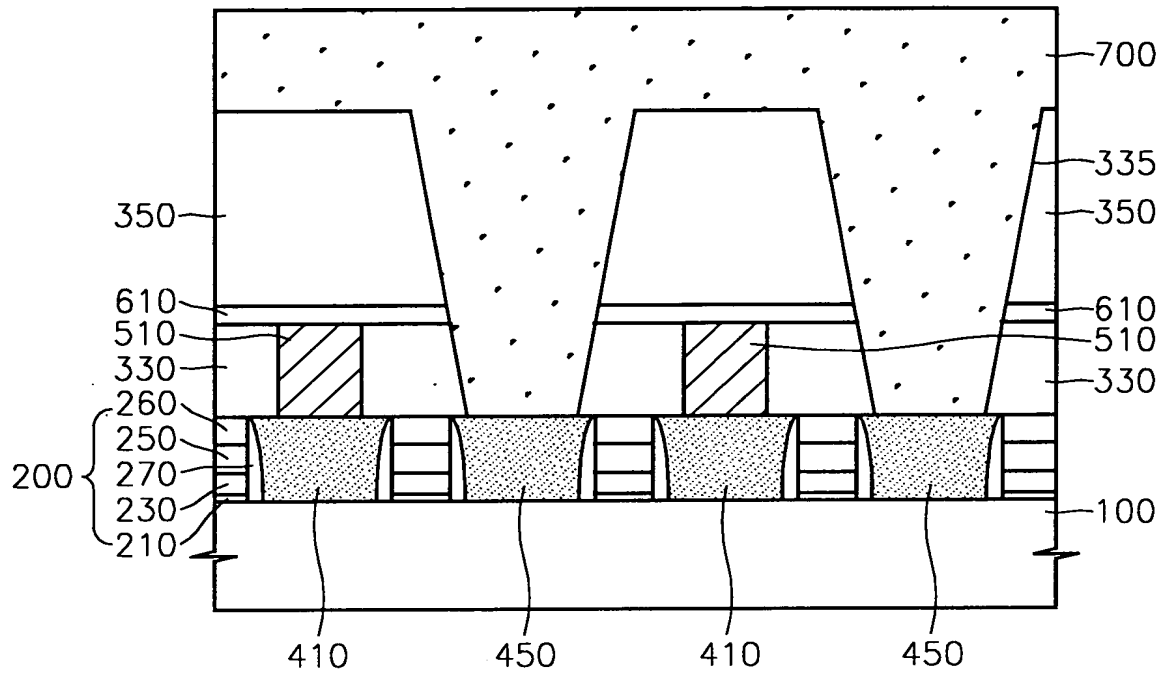


Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 100. A gate stack 200 is formed on the substrate 100. The gate stack 200 includes a gate 350, a gate dielectric layer 330, a gate conductive layer 510, and a gate insulating layer 610. A channel 410 is formed in the substrate 100, and a source/drain region 450 is formed in the substrate 100. A contact 800 is formed in the substrate 100.

FIG. 3B

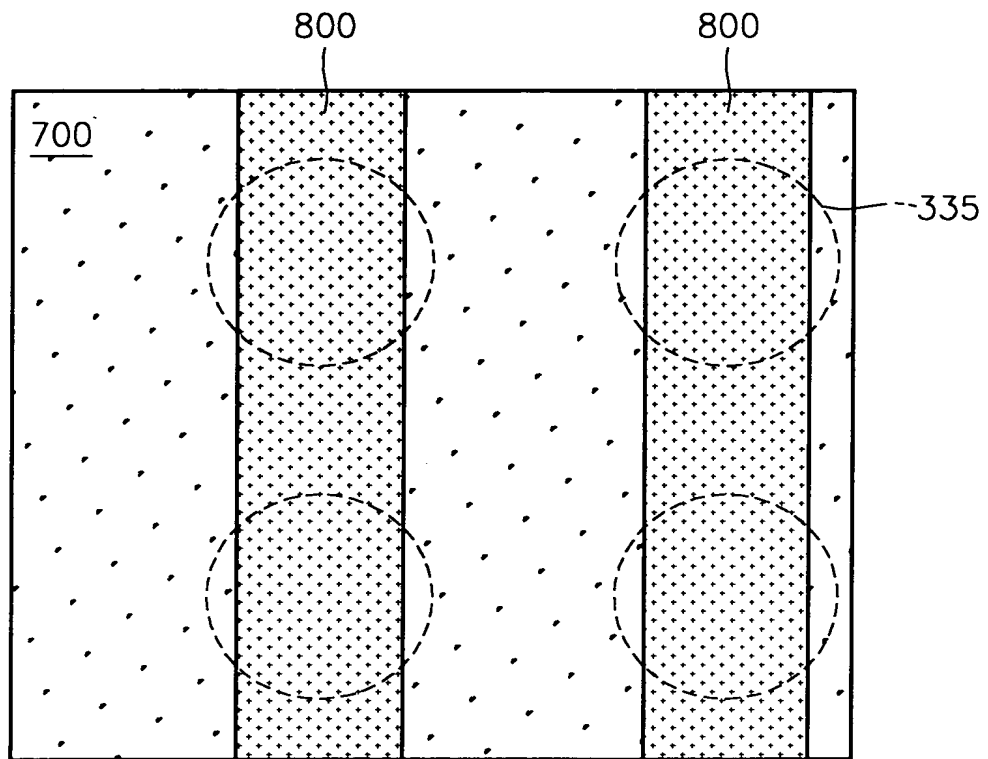


FIG. 4A

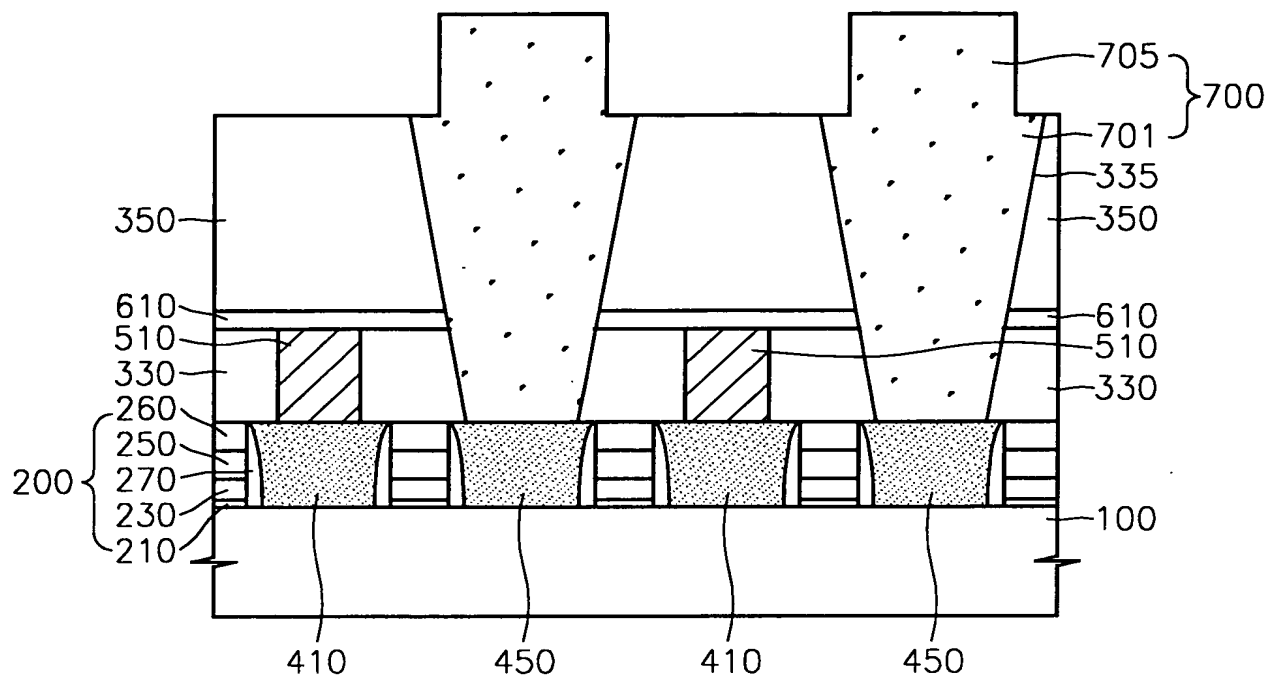


FIG. 4B

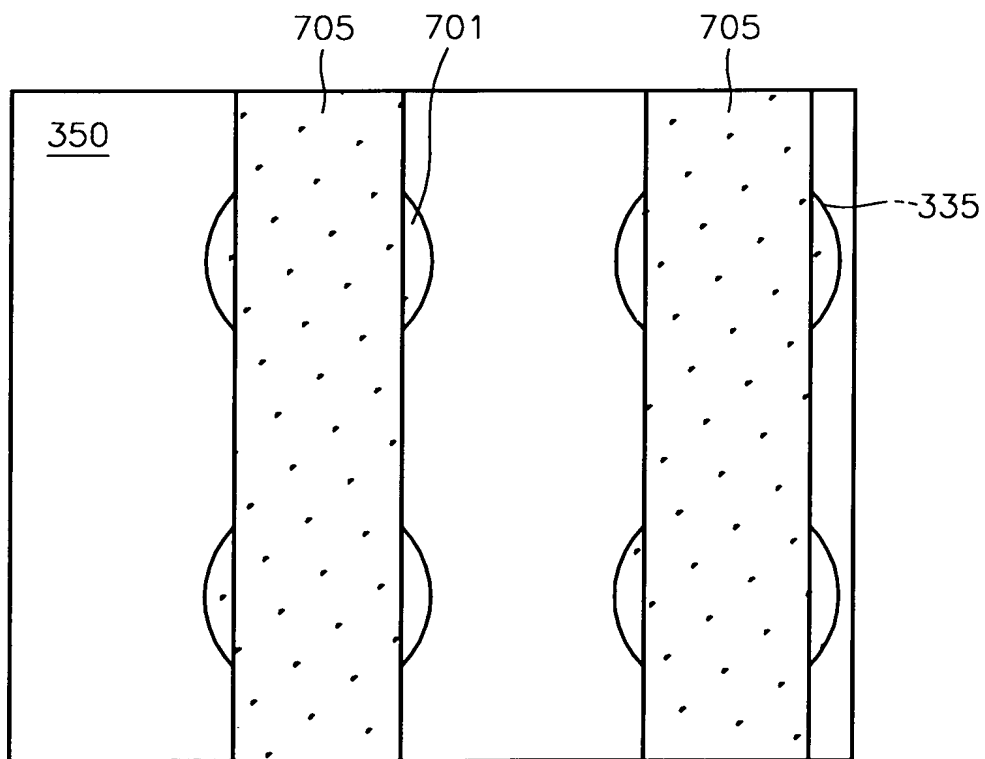


Figure 1 is a cross-sectional view of a semiconductor device 100. The device 100 includes a substrate 210, a device layer 230, and a protective layer 350. The device layer 230 contains a series of rectangular blocks 250 and 270. Above these blocks are various layers including 260, 330, 510, and 610. The device is surrounded by a protective layer 350 and a top layer 705. The top layer 705 is divided into regions 701 and 705. The device is also labeled with 337 and 351.

The diagram illustrates two states of a device. On the left, a central region labeled 330 is bounded by vertical dashed lines. It is surrounded by regions 350 and 705. A circular feature with diagonal hatching, labeled 510, is positioned to the left of the central region. On the right, a similar structure is shown, but with a curved arrow pointing from the central region towards a new position, labeled 335, which is indicated by a dashed line. Other labels include 350, 705, and 701.

FIG. 6A

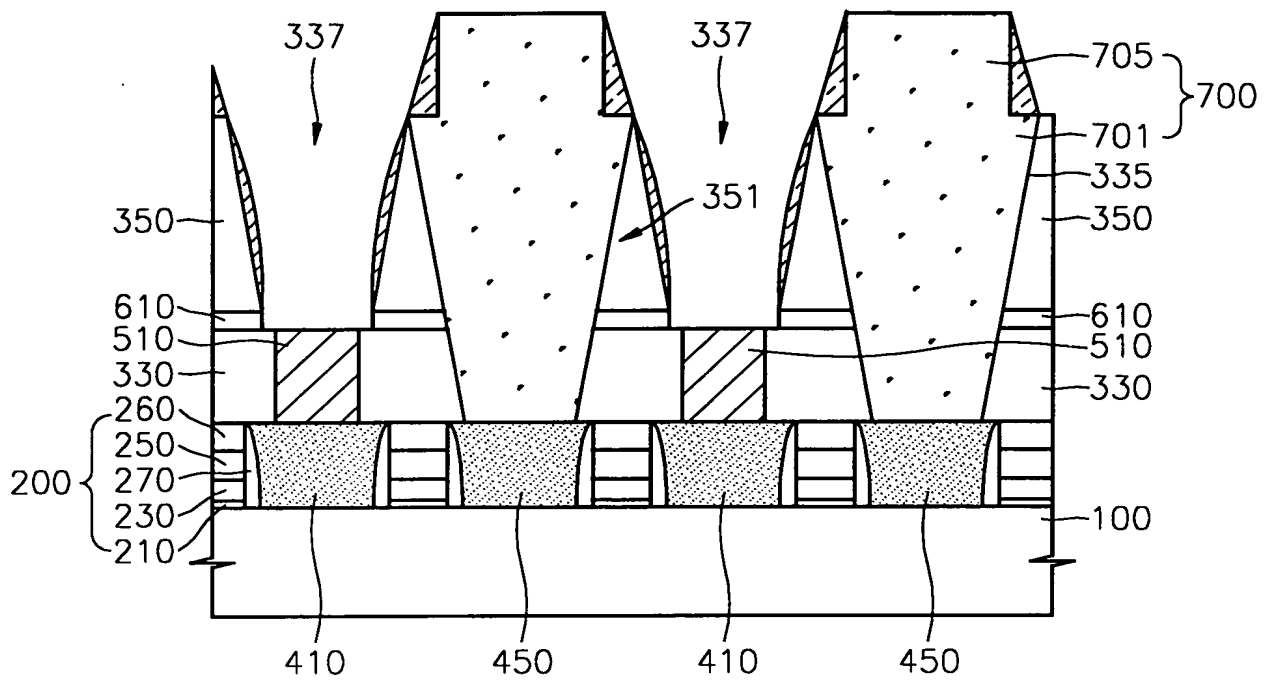


FIG. 6B

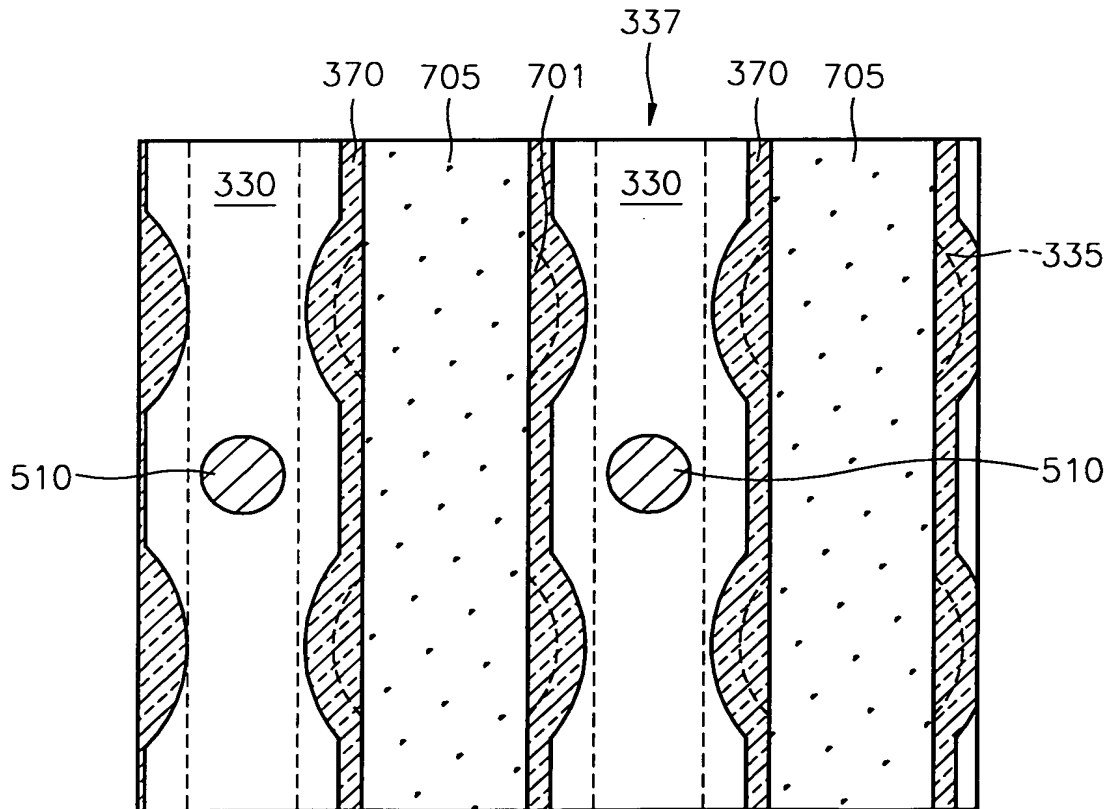


FIG. 7

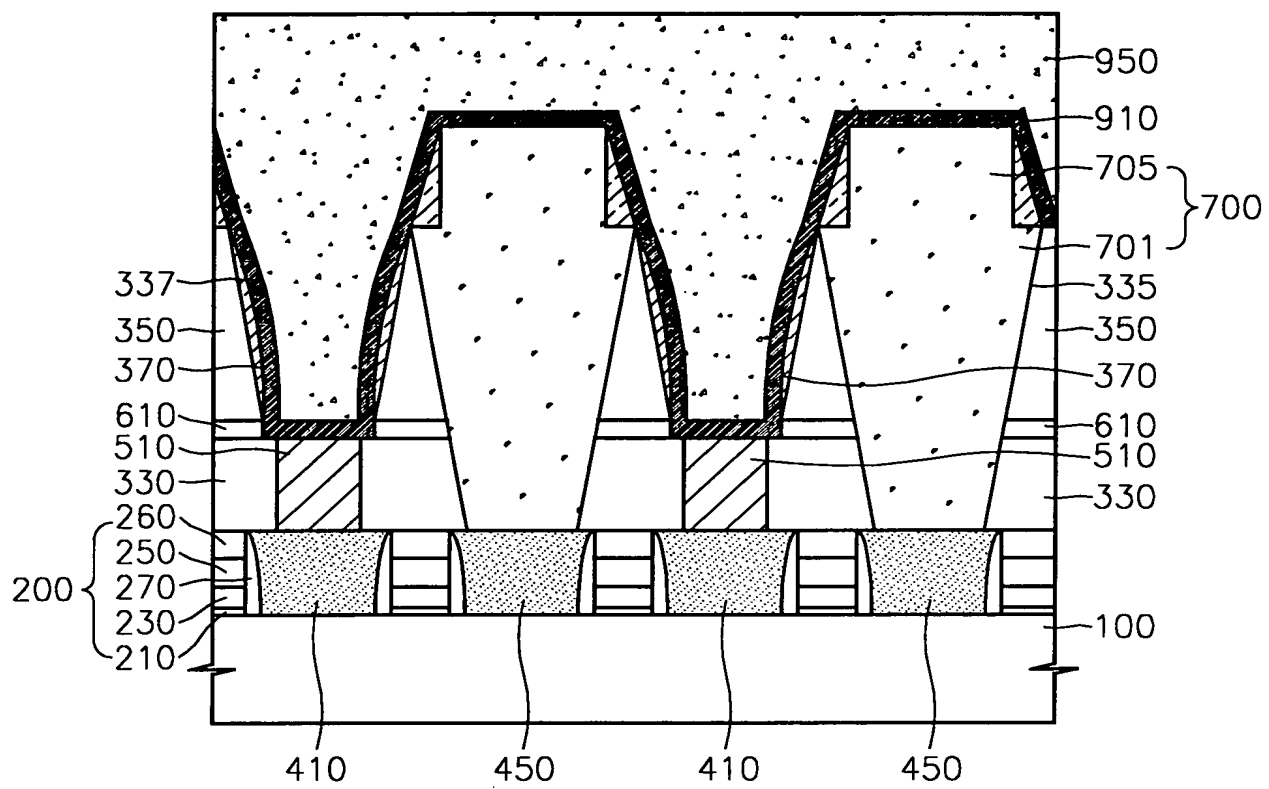


FIG. 8A

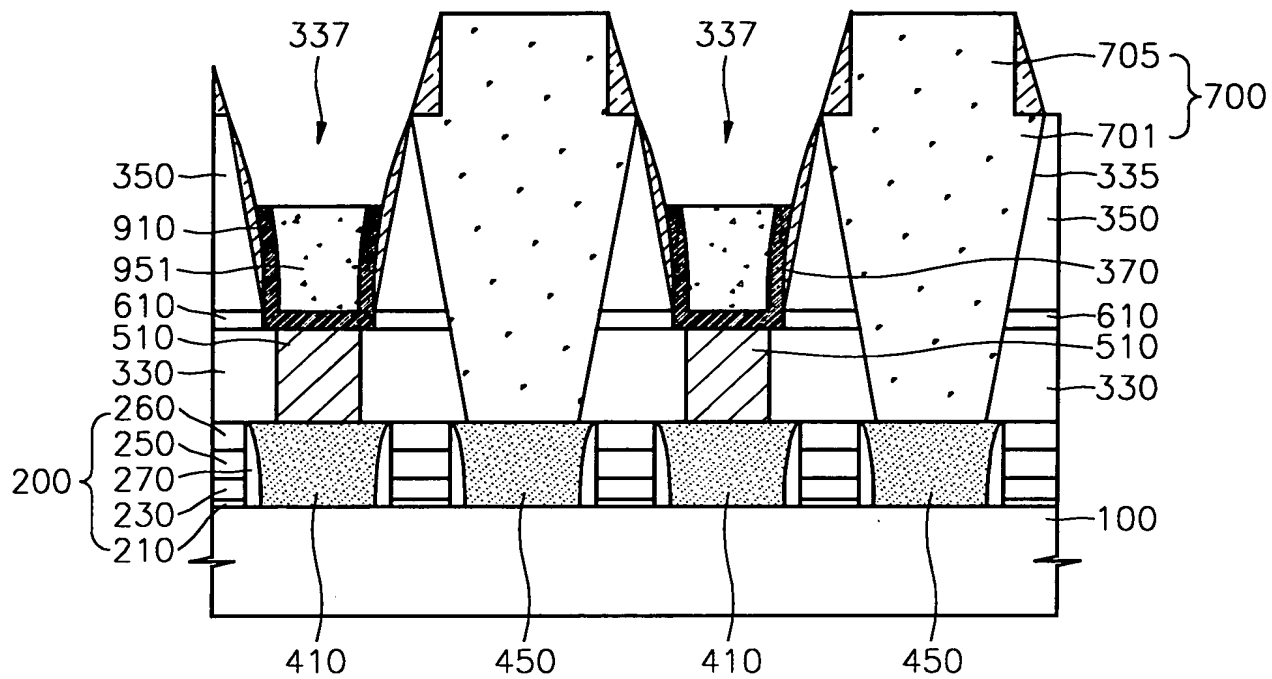


FIG. 8B

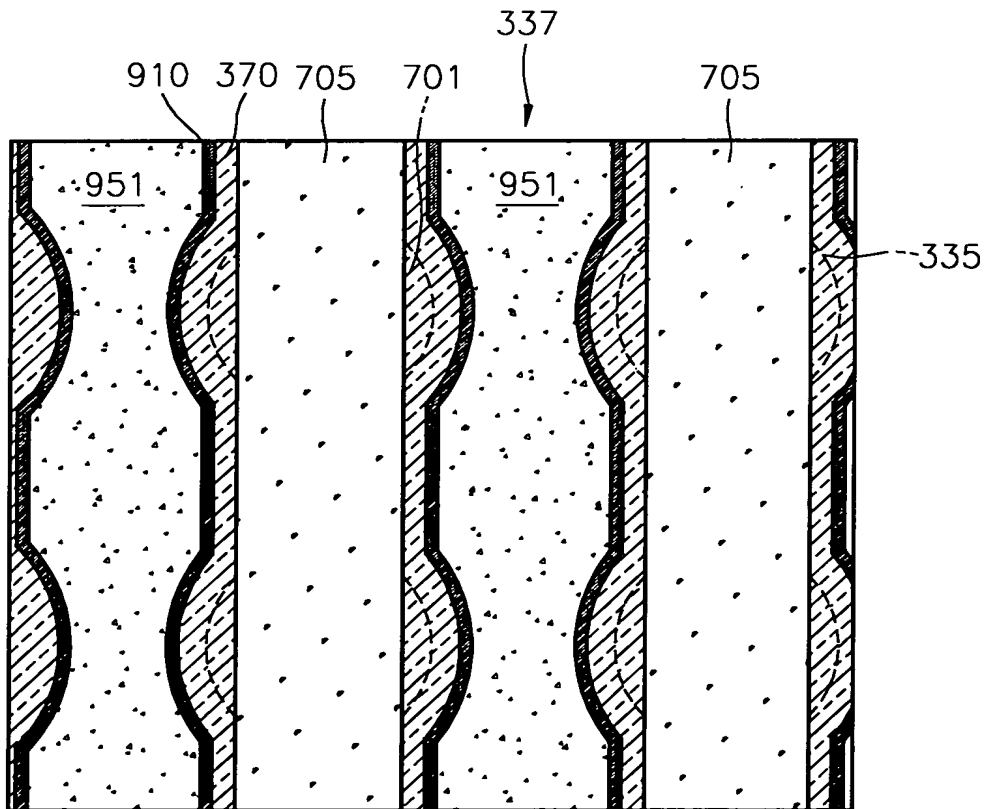


FIG. 9

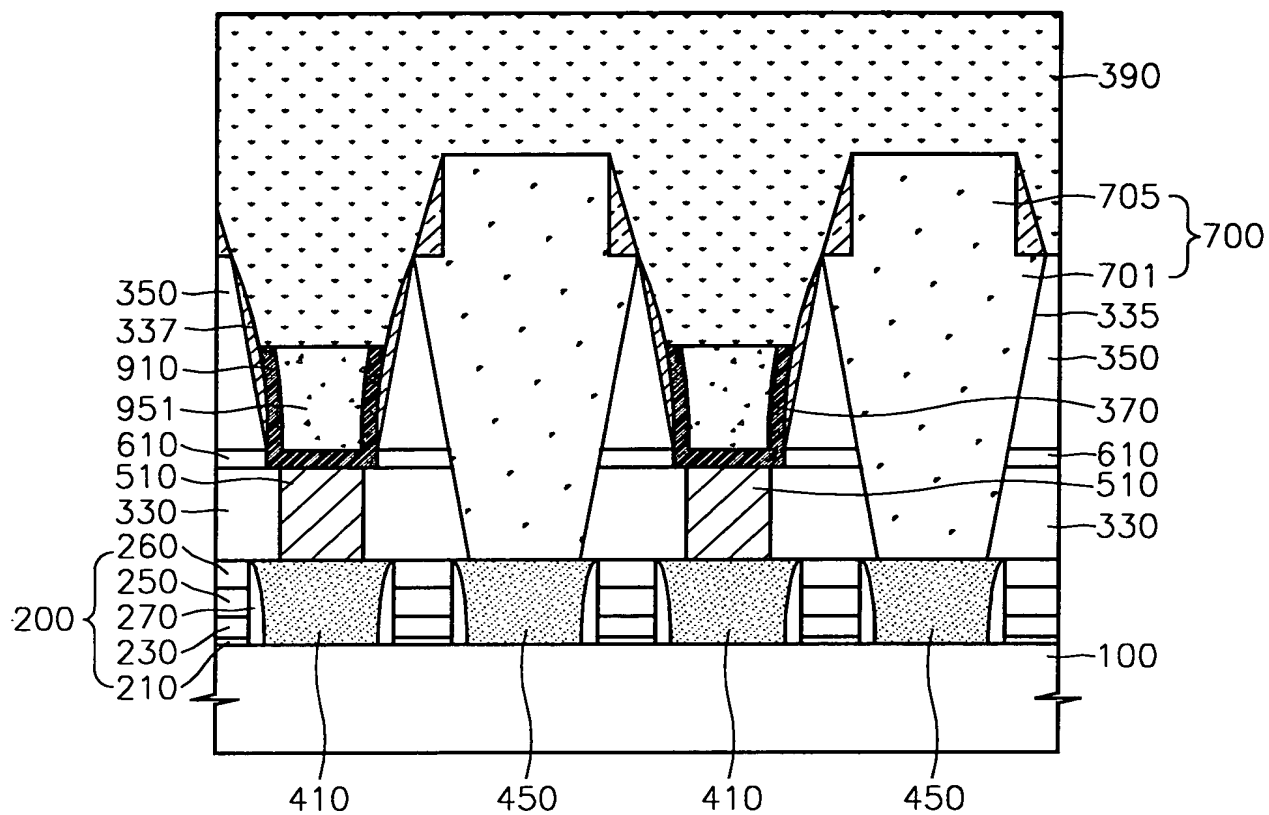


Figure 1 is a schematic diagram of a substrate 350. The substrate is a rectangular block with a grid of circular features 390. The features are arranged in a 2x2 grid. A cross-section line 701 is indicated on the right side of the substrate.

FIG. 11

